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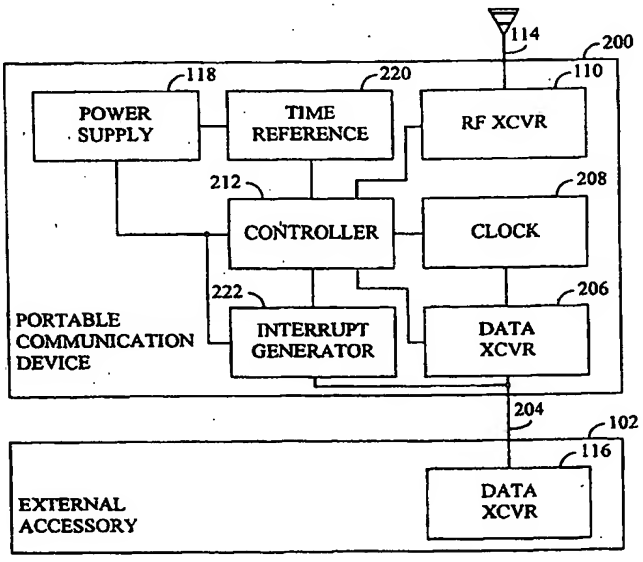

(57) Abstract

A portable communication device (200) selectively enables and disables a data transceiver (206), controller (212), and clock (208) in response to the presence or absence of data on a data port (204). A data transceiver (206) detects a break condition on the data port. A controller (212) disables the data transceiver (206) in response to the break condition detection, and arms an interrupt generator (222) which monitors the data port (204) while the data transceiver (206) is disabled. The interrupt generator (222) detects a transition from the break condition to an idle condition, and generates an interrupt signal in response thereto. The controller (212) enables the data transceiver (206) and clock (208) in response to the interrupt signal.

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METHOD AND CIRCUIT FOR ENABLING AND DISABLING A DATA TRANSCEIVER

BACKGROUND OF THE INVENTION

I. Field of the invention

The present invention relates to data transceivers. More specifically, the present invention relates to a method and circuit for enabling and disabling a data transceiver based on the detection of a data transition on the data transceiver data input.

II. Description of the Related Art

In the field of portable communication devices such as wireless telephones, pagers, palmtop computers, data organizers and the like, the portable communication device is typically powered by batteries. It is well understood that the capacity of these batteries is dependent upon the power consumption of the portable communication devices. Intuitively, the power consumption at any given time depends on how many and what type of components inside the portable communication device are powered on and operating.

Because batteries have a finite capacity, it is often desirable to partially "power-down" unused components or circuits within the portable communication device in order to save battery power. For example, it is well known in the art to remove power from a wireless telephone's radio transmission circuitry when it is not actively transmitting, thereby saving power that would otherwise be wasted. Likewise, it is well known to remove power from the wireless telephone's radio reception circuitry when no signals of interest are expected to be received, such as during non-assigned paging slots.

In general, it is understood that the less circuitry operating at any given time, the less battery power will be consumed by the portable communication device, thereby increasing its overall battery life. However, it is also understood that when

the powered-down circuitry is suddenly needed to perform its function, it must be "powered-up" promptly and reliably. For this reason, it is necessary to be able to reliably determine when to re-enable circuitry that has been previously disabled for power saving purposes.

Many portable communication devices are equipped with data ports which may be used to interface with various external accessories such as a hands-free car kit, a personal computer, or other user terminal. These data ports are typically driven by a data transceiver such as a Universal Asynchronous Receiver Transmitter (UART) or similar device. When the portable communication device is not actually communicating with an external accessory through the data port, it would be advantageous to disable the UART and its associated timing and control circuitry to save battery power.

An example functional block diagram of a prior art portable communication device 100 and external accessory 102 is illustrated in FIG. 1. For example, the portable communication device 100 may be a wireless telephone and the external accessory 102 may be a hand-free car kit. In operation, radio frequency (RF) signals are transmitted and received by RF transceiver (RF XCVR) 110 over antenna 114. On the other hand, data signals are transmitted and received by data transceiver 106 over data port 104 with transceiver 116 in the external accessory 102. In a typical application, these data transceivers 106 and 116 will be UARTs operating according to the RS-232 Serial Communication Standard as is well known in the art.

Clock 108 provides the clock signal necessary for RS-232 serial communications to data transceiver 106. A power supply 118 supplies power to controller 112, RF transceiver 110, clock 108, and data transceiver 106. Power supply 118 may be, for example, a rechargeable battery and associated voltage or current generation circuitry as is known in the art.

In order to minimize power consumption when the external accessory 102 is not connected, it is desirable to power down the data transceiver 106, and even unneeded portions of controller 112 and clock 108. Unfortunately, when the data transceiver 106 and its associated clock 108 and controller 112 are disabled, the data transceiver 106 is unable to detect the presence of incoming data at the data port

104. As such, it is unable to "wake up" when needed to process incoming data on the data port 104. This prevents the prior art portable communication device 100 of FIG. 1 from being able to power down the data transceiver 106, clock 108 and controller 112 when the data transceiver 116 in the external accessory 102 is not transmitting.

What is needed is a method and circuit for reliably enabling and disabling a data transceiver and its associated timing and control circuitry to allow for power-savings when the data port is not being actively used.

SUMMARY OF THE INVENTION

The present invention is a novel and improved method and circuit for saving power in a portable communication device by selectively enabling and disabling a data transceiver in the portable communication device in response to the presence or absence of data on a data port of the portable communication device.

In one aspect of the present invention, the portable communication device has a data port for communicating with an external accessory. A data transceiver, coupled to the data port, communicates data over the data port. The data transceiver also detects a break condition on the data port. A break condition corresponds to a lack of information being communicated.

A controller, coupled to the data transceiver, disables the data transceiver in response to the break condition detection and arms an interrupt generator which, monitors the data port while the data transceiver is disabled. The interrupt generator detects a transition from the break condition to an idle condition and generates an interrupt signal in response thereto. The controller enables said data transceiver in response to the interrupt signal.

In another aspect of the present invention, the controller partially powers down in response to the break condition detection and wakes up in response to the interrupt signal.

A clock, coupled to the controller and the data transceiver, generates a clock signal for use by the controller and the data transceiver. Optionally, the controller

also disables the clock in response to the break condition detection, and enables the clock in response to the interrupt signal.

When no data is actually being transmitted on the data port, the portable communication device saves power and increases battery life by disabling the data transceiver, the controller, and optionally, the clock. However, the interrupt generator provides reliable re-enabling of the data transceiver, controller, and clock when they are necessary for data transmission.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. I is a functional block diagram of a prior art portable communication device and external accessory system;

FIG. 2 is a functional block diagram of an exemplary embodiment of the portable communication device and external accessory system of the present invention;

FIG. 3 is a timing diagram of an exemplary data signal present at the data port of the portable communication device of FIG. 2; and

FIG. 4 is a flow diagram of the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although the present invention will be described herein with reference to an exemplary embodiment in a wireless communication device, it is understood that the principles described herein will apply equally to other portable electronic devices that communicate data with an external entity. For example, the present invention is generally applicable to portable computers such as laptop computers and palmtop computers. The present invention is also applicable to electronic data organizers such as day planners, data gatherers such as bar code readers, or

inventory managers and the like. Broadly, the present invention is applicable to any portable electronic device which communicates data with an external accessory.

Referring now to FIG. 2, a functional block diagram of an exemplary embodiment of the present invention as used in a wireless communication device 200 is illustrated. Antenna 114, RF transceiver 110, power supply 118, external accessory 102 and data transceiver 116 are identical to like-numbered elements in FIG. I.

In FIG. 2, wireless communication device 200 is shown as being coupled to external accessory 102 through data port 204. Data transceiver 206 transmits and receives data over data port 204 to and from data transceiver 116. Data transceivers 206 and 116 may generally be any data transceiver as is known in the art including UART as are commonly available from many suppliers. Alternately, data transceiver 206 may be integrated into an Application Specific Integrated Circuit (ASIC) along with other components shown in FIG. 2. In the exemplary embodiment of FIG. 2, data transceivers 206 and 116 communicate according to the well-known RS-232 Serial Communication Standard.

A clock 200 generates timing signals according to well-known principles for use by data transceiver 206 and controller 212. Clock 208 may be a crystal oscillator with associated clock signal generation circuitry. For example, clock 208 may be a Temperature-Compensated Crystal Oscillator (TCXO), or a voltage Controlled, Temperature-Compensated Crystal Oscillator (VCTCXO) with the associated digital signal conditioning components as are well known in the art for digital clock signal generation. Controller 212 is coupled to clock 208 and data transceiver 206, and selectively enables and disables them as will be described further below. Controller 212 may be any suitable microprocessor or microcontroller as is known in the art, programmed with software for performing the steps described herein. Alternatively, controller 212 may be implemented in discrete logic, or a combination of discrete logic, integrated circuitry, and software. Controller 212 may also be integrated into an ASIC device along with data transceiver 206.

Power supply 118, which may be one or more battery cells and associated voltage or current generation circuitry, is coupled to each of the components of

portable communication device 200. The RP transceiver 110, clock 208, and data transceiver 206 are each capable of being selectively enabled by applying or removing power from them. As such, power for these components is routed through the controller 212 which functions to selectively switch power to these components when they must operate, and to switch power away (i.e., power them down) when they are not required to operate.

An interrupt generator 222 is also shown in FIG. 2 as being coupled to the data port 204 and the controller 212. Interrupt generator 222 senses a transition in the data present at data port 204 and generates an interrupt to controller 212 in response, as will be described further below. Interrupt generator 222 may be any circuit as is known in the art for detecting a transition on a digital data line, and generating an interrupt in response. Thus, interrupt generator 222 may be discrete digital logic, a microprocessor programmed with appropriate. software, or any combination of similar elements.

Also shown in FIG. 2 is a time reference 220 coupled to controller 212. Time reference 220, like clock 208 may be a crystal oscillator. Alternately, time reference 220 may be a low-power reference such as a 32 Khz crystal oscillator commonly available for less accurate applications such as watches. It should be noted that in one embodiment wherein clock 208 is not powered down, the separate time reference 220 is not required.

In the exemplary embodiment of FIG. 2, data transceivers 206 and 116 communicate over data port 204 using the RS-232 serial communication standard. The present invention is equally applicable to other data communication standards, whether or not serial in nature, including the universal Serial Bus standard. However, for the purpose of simplicity and clarity, the present invention will be described with reference to an exemplary RS-232 communication scheme.

According to the RS-232 standard, binary data (i.e., ones and zeros) are represented by "marking" and "spacing" conditions. These marking and spacing conditions are defined by the voltage levels on the RS-232 interface, here data port 204. According to section 2.1.3 of the RS-232 standard, the signal is considered in the marking condition when the voltage on the interface is more negative than --3 volts with respect to signal common (i.e., ground). Similarly, spacing is when the

voltage on the interface is more positive than +3 volts with respect to signal common. During the transmission of data, the marking condition is used to denote the binary state 1, and the spacing condition is used to denote the binary state 0.

Under the RS-232 standard, the external data transceiver 116 holds the transmitted signal to the portable communication device 200 in the marking condition at all times when no data is being transmitted. This is often referred to as being in the "idle" state. Additionally, a "break" can be signaled by the external data transceiver 116 holding the transmitted signal in the spacing condition for a predetermined time period.

Although the terms "marking", "spacing", "break" and "idle" are defined in RS-232, those terms are used herein to correspond to data states or conditions generally, without respect to the specific limitations of RS-232. The terms "marking" and "spacing" as used herein refer to signaling binary information using different logic levels. The terms "break" and "idle" as used herein refer to holding the logic level at one level or the other for an indefinite period of time without actually transmitting informational binary data.

This mark/space and break/idle transitioning is illustrated in FIG. 3. FIG. 3 represents an example of the data signal that is present on the data port 204. FIG. 3 illustrates a graph of the voltage level (V) present on the data port 204 over time. During a first time period 302, the voltage level is above +3 volts. This first time period corresponds to a spacing or break condition. This is the expected initial state of the data port 204 when no external accessory is connected due to the data transceiver 206 pulling the data port 204 to a logic level zero (i.e., spacing condition) when there is no connection. It is understood that in other embodiments data transceiver 206 may instead pull the data port 204 to a logic level one when there is no connection.

Upon connection of external accessory 102 to the data port 204, data transceiver 116 will, according to the RS-232 standard, transition the data signal on the data port 204 from the spacing or break condition 302 to the marking or idle condition 304. The marking or idle condition 304, as explained above, corresponds to the data transceiver 116 being connected, but not transmitting any data information. This transition from break 302 to idle 304 is represented by the falling

edge 303. This falling edge is detectable by interrupt generator 222 (FIG. 2), as will be discussed further below.

During time periods 306, data transceiver 206 and data transceiver 116 exchange data over data port 204, as represented by the voltage level (V) of FIG. 3 transitioning between marking and spacing conditions according to the data being transmitted. Upon completion of the exchange of data, data transceiver 116 will again hold the data port 204 in the marking condition at time period 308, signifying an idle condition.

In other embodiments, the polarity of the logical ones and zeros may be reversed, i.e. the marking condition may represent a logic level zero, and the spacing condition may represent a logic level one. Additionally, the interrupt generator 222 may be configured to detect a rising edge rather than a falling edge. It will be understood by one of ordinary skill in the art that the present invention is not limited by the direction of the transition (e.g., rising/falling edge) or by the polarity of the logic levels.

Referring now to FIG. 4, a flowchart of the method of the present invention with respect to the exemplary embodiment of FIG. 2 is illustrated. The method begins at block 402 where the data transceiver 206 monitors the data port 204 for data. If the data transceiver 206 does not detect a break condition on the data port 204 at decision 404 (i.e., data is actively being transmitted), the data transceiver 206 continues to monitor data port 204 normally.

If, on the other hand, the data transceiver 206 detects a break condition on the data port 204 at decision 404, the data transceiver 206 signals this break condition to controller 212, and controller 212 arms interrupt generator 222 in response at block 406. As explained above, a break condition signals that the external accessory has been disconnected or is otherwise disabled from transmitting data. At block 408, controller 212 disables data transceiver 206 by removing power from at least a portion of the data transceiver 206. This step is also referred to herein generally as "powering down" the data transceiver 206, thereby saving battery power.

At block 410 (shown in dashed lines), controller 212 optionally disables clock 208 by removing power from at least a portion of the clock 209. This step is shown

as optional because in some embodiments, where a separate time reference 220 is not used, the clock 206 may not be disabled. However, where a separate, lower-power time reference 220 is available, additional power savings may be had by disabling clock 208 at block 410.

At block 412, controller 212 powers down by removing power from non-essential portions. Thus, at this point in the process, data transceiver 206, controller 212 and optionally clock 208 are in a power-saving mode, leaving interrupt generator 222 to monitor the data port 204 at block 414. Because the total power consumption of the circuitry of interrupt generator 222 is less than the combined power consumption of controller 212 and data transceiver 206, a net power savings is achieved.

Interrupt generator 222 continues to monitor data port 204 until it detects a break-to-idle transition at decision 416. As explained above, the break-to-idle transition is used by the external data transceiver 116 to signal that a connection has been made. When interrupt generator 222 detects the break-to-idle transition, it generates an interrupt signal to controller 212 at block 418. In response to receiving the interrupt signal, controller 212 "wakes up" (i.e., reapplies power to its necessary circuitry) at block 420.

If clock 208 was disabled at block 410, then it is re-enabled at block 422. Also, at block 422, controller waits a predetermined time period for the clock 208 to stabilize. Clock stabilization periods after power-up are well known in the art and are a function of the clock design.

At block 424, the controller enables the data transceiver 206, and the flow returns to block 402 where the data transceiver 206 continues to monitor the data port 204 normally.

Thus, the present invention allows the data transceiver 206, controller 212, and optionally, clock 208 to reduce their power consumption when no actual data is being transmitted on data port 204, while still enabling normal data communications on data port 204 when needed. In this way, the present invention contributes to an increase in battery life in portable communication devices.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The

various m[illegible]cations to these embodiments will be readily apparent to those skilled in th[illegible]t, and the generic principles defined herein may be applied to other embodiments without the use of inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WE CLAIM:

CLAIMS

1. A portable communication device having a data port for communicating with an external accessory, the portable communication device comprising:

a data transceiver, coupled to said data port, for communicating data over said data port, and for detecting a break condition on said data port;

a controller, coupled to said data transceiver, for disabling said data transceiver in response to said break condition detection; and

an interrupt generator, coupled to said data port and said controller, for detecting a transition from said break condition and for generating an interrupt signal in response thereto;

wherein said controller enables said data transceiver in response to said interrupt signal.

2. The portable communication device of claim 1 wherein said controller partially powers down in response to said break condition detection.

3. The portable communication device of claim 2 wherein said controller wakes up in response to said interrupt signal.

4. The portable communication device of claim 3 further comprising:

a clock, coupled to said controller and said data transceiver, for generating a clock signal;

and wherein said controller disables said clock in response to said break condition detection.

5. The portable communication device of claim 4 wherein said controller enables said clock in response to said interrupt signal.

6. A method for saving power in a portable communication device having a data transceiver for communicating with an external accessory over a data port, the method comprising the steps of:

communicating data over said data port;

detecting a break condition on said data port;

disabling said data transceiver in response to said step of detecting said break condition;

detecting a transition from said break condition;

generating an interrupt signal in response to said detecting a transition step; and

enabling said data transceiver in response to said interrupt signal.

7. The method of claim 6 further comprising the step of partially powering down a controller in said portable communication device in response to said step of detecting said break condition.

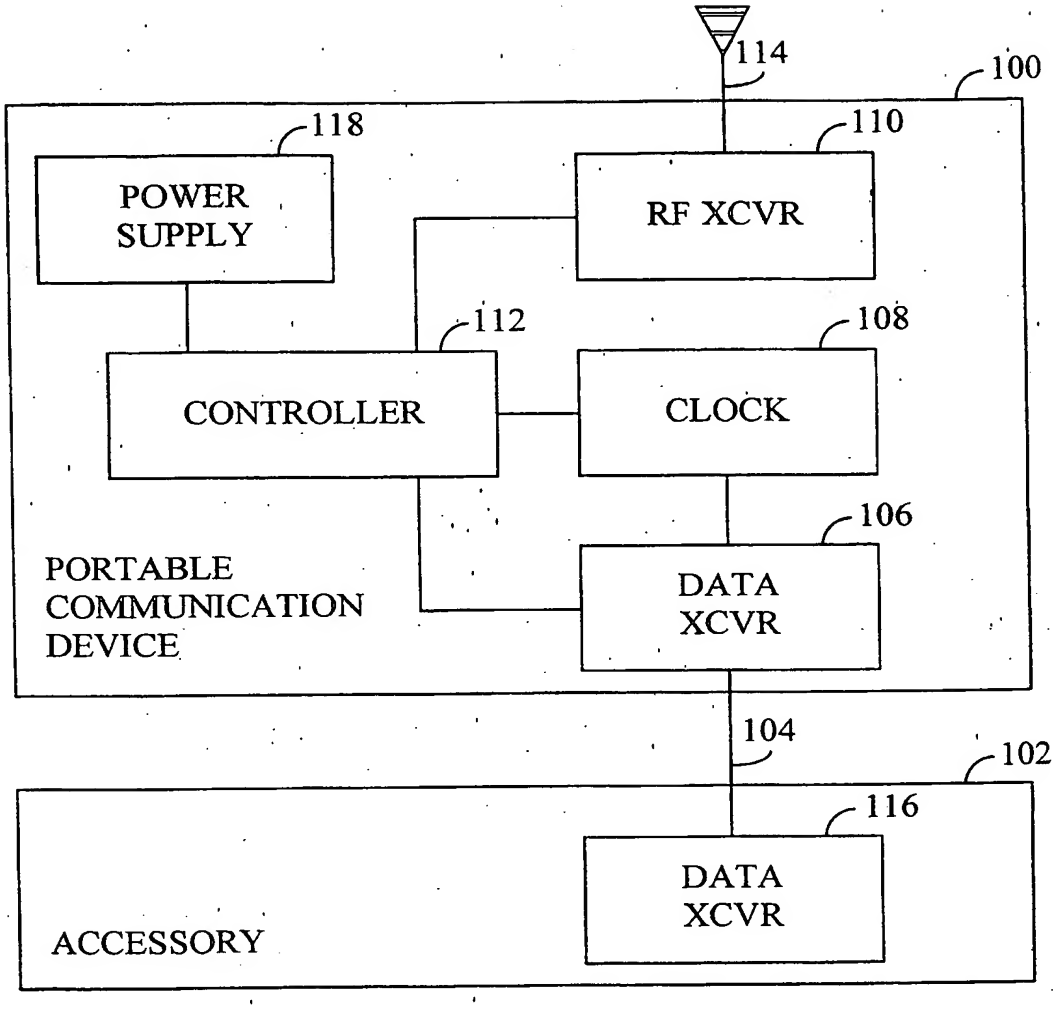
8. The method of claim 7 further comprising the step of waking up said controller in response to said interrupt signal.

9. The method of claim 8 further comprising the steps of:

generating a clock signal; and

disabling said clock signal generation in response to said step of detecting said break condition.-...

10. The method of claim 9 further comprising the step of enabling said clock signal generation- in response to said interrupt signal.


114
100
118
110
POWER SUPPLY
RF XCVR
112
108
CONTROLLER
CLOCK
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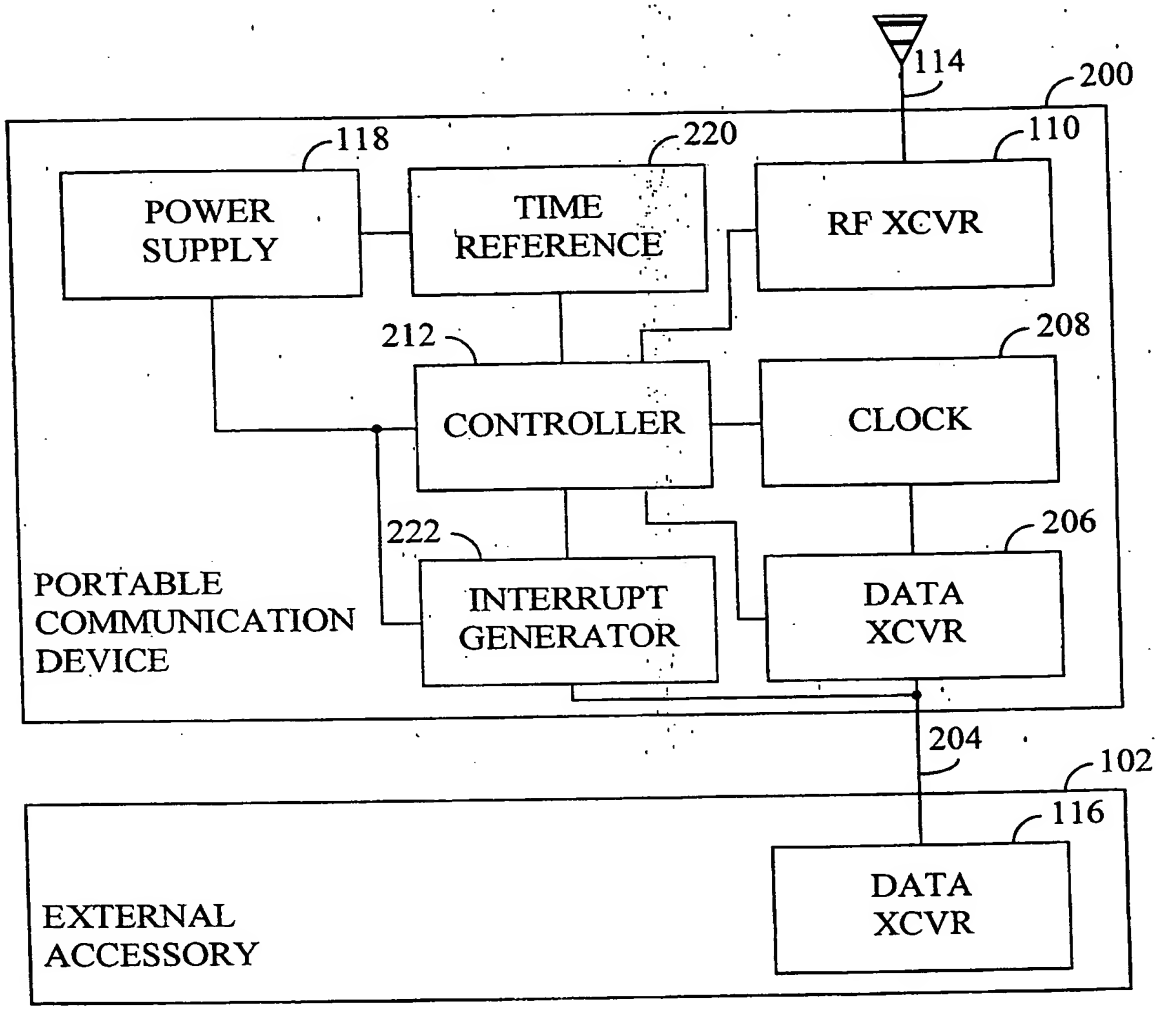
PORTABLE COMMUNICATION DEVICE
DATA XCVR
104
102
116
DATA XCVR
ACCESSORY

FIG. 1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200
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POWER SUPPLY
TIME REFERENCE
RF XCVR
212
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CONTROLLER
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INTERRUPT GENERATOR
DATA XCVR
204
102
116
DATA XCVR
EXTERNAL ACCESSORY

FIG. 2

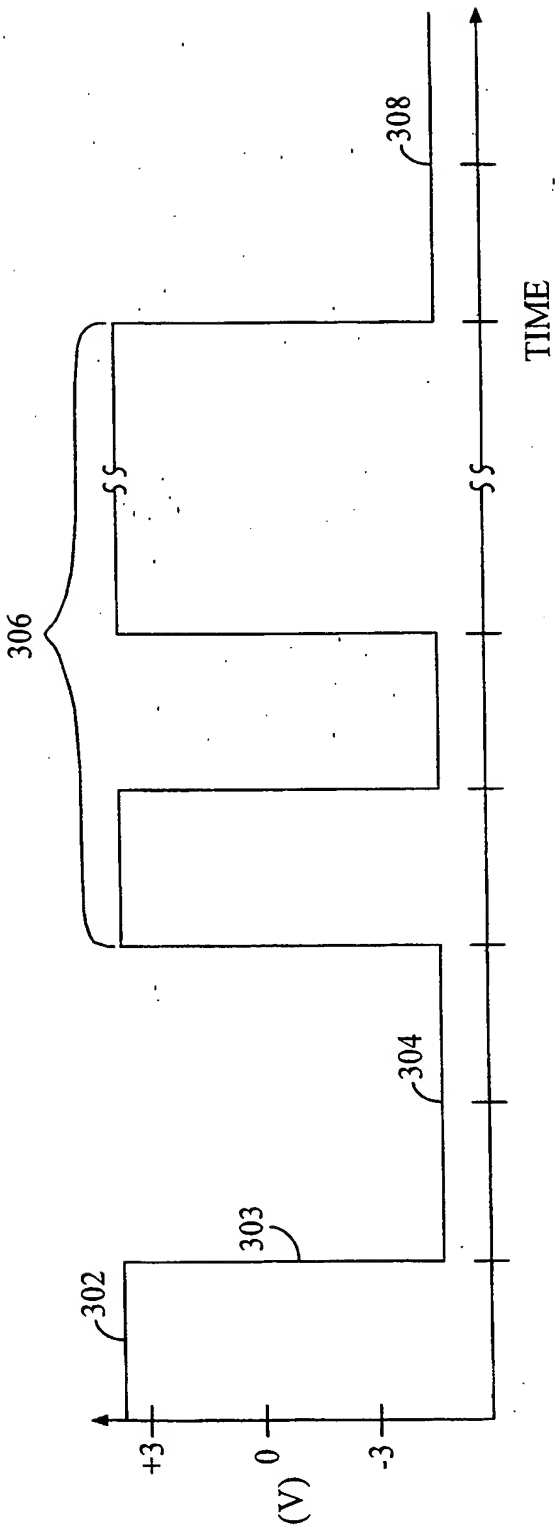

FIG. 3

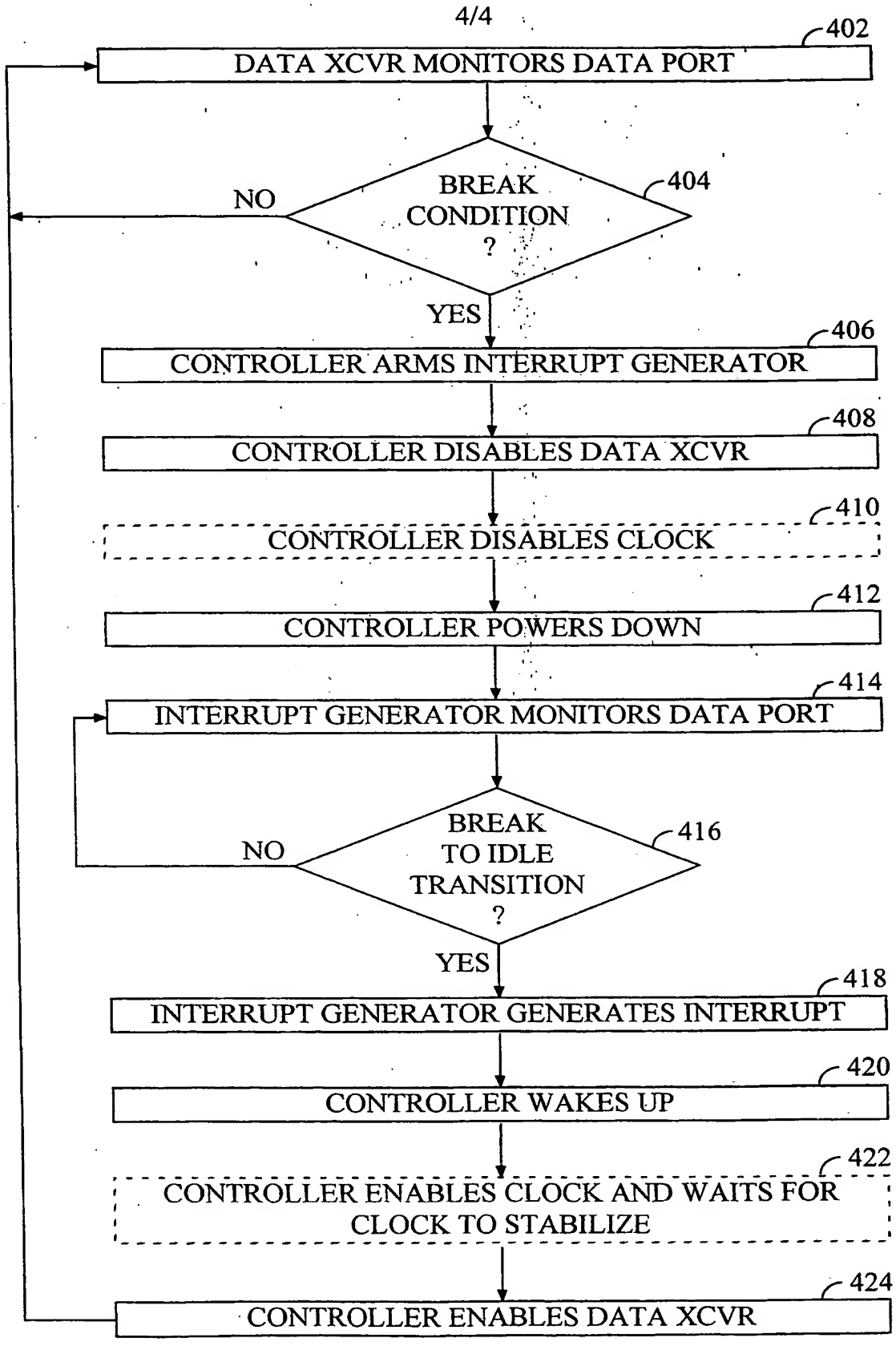
402
DATA XCVR MONITORS DATA PORT
404
BREAK CONDITION ?
NO
YES
406
CONTROLLER ARMS INTERRUPT GENERATOR
408
CONTROLLER DISABLES DATA XCVR
410
CONTROLLER DISABLES CLOCK
412
CONTROLLER POWERS DOWN
414
INTERRUPT GENERATOR MONITORS DATA PORT
416
BREAK TO IDLE TRANSITION ?
NO
YES
418
INTERRUPT GENERATOR GENERATES INTERRUPT
420
CONTROLLER WAKES UP
422
CONTROLLER ENABLES CLOCK AND WAITS FOR CLOCK TO STABILIZE
424
CONTROLLER ENABLES DATA XCVR

FIG. 4

INTERNATIONAL SEARCH REPORT

Interr. ...al Application No
PCT/US 99/17306

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04M1/72

According to International Patent Classification (IPC) or to both national classification and IPC

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20 October 1999	28/10/1999

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern. nal Application No
PCT/US 99/17306

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